SQUARING CELLS AND MULTIPLIERS USING SUMMED EXPONENTIALS

5   This application is a continuation of prior application Serial No. 10/192,115, filed July 9, 2002, which is a divisional of prior application Serial No. 09/473,309, filed December 28, 1999, which is now U.S. Patent No. 6,437,630, which are herein incorporated by reference; this application is also a divisional of prior application Serial No. 10/319,368, filed 10   December 12, 2002, which is a divisional of prior application Serial No. 10/170,067 filed June 11, 2002, which is a divisional of prior application Serial No. 09/569,544 filed May 12, 2000, which is now U.S. Patent No. 6,429,720B1 issued August 6, 2002, which are herein incorporated by reference.

15   BACKGROUND OF THE INVENTION

        1.   Field of the Invention

         The present invention relates generally to RMS-DC converters, and more particularly, to RMS-DC converters, which utilize gain stages and variable weighting coefficients to provide a very wide measurement range.

20   2.   Description of the Related Art

         RMS-DC converters are used to convert the RMS (root-mean-square) value of an arbitrary signal into a quasi-DC signal that represents the true power level of the signal. Various techniques have been devised for performing RMS-to-DC conversions at frequencies ranging from DC to several GHz, some of which are disclosed in co-pending U.S. Patent 25   Application Nos. 09/245,051 filed February 4, 1999, which is now U.S. Patent No. 6,204,719, and 09/256,640 filed February 24, 1999, which is now U.S. Patent No. 6,172,549, which are by the same inventor as the present application, and are incorporated herein by reference.

         Performing accurate RMS-DC conversions over a wide dynamic range has proven 30   difficult, especially at RF frequencies of several GHz. The need for wide dynamic range true-power measurement at very high frequencies has become more critical because the signals generated by modern communications systems such as those using CDMA have very wide instantaneous bandwidth and complex waveforms, with high crest factors, and because operating frequencies are continuously being pushed higher.

35   Logarithmic amplifiers (log amps) are often used to measure the power of RF signals because they can provide a good indication of power over a very wide bandwidth, but the

measurement depends on the waveform of the RF signal. Synchronous log amps are of special interest in this regard because they reduce the noise floor compared to other log amps, and therefore, provide extended dynamic range. A synchronous log amp is disclosed in U.S. Patent No. 5,298,811 which issued to the inventor of the present application and which are

5   incorporated by reference.

However, logarithmic amplifiers, including synchronous log amps, do not provide an RMS response. When a signal of substantial amplitude is applied to a log amp, most of the amplifier cells operate in a limiting mode, which precludes the attainment of a square-law response in the constituent detector cells, or in the sum of their outputs.

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SUMMARY

In one aspect of the present invention, a series of cascaded gain stages generate a series of progressively amplified signals, which are squared and weighted and then summed to provide a true square-law response. In another aspect of the present invention, two parallel

15   series of cascaded gain stages generate a series of progressively amplified signal pairs, which are multiplied and weighted and then summed to provide a true square-law response while also canceling uncorrelated noise. In a further aspect of the present invention, two signals are generated by exponential signal generators responsive to an input signal, and combined to provide an output signal, which approximates the squared value of the input signal. In

20   another aspect of the present invention, four signals are generated by exponential signal generators responsive to two input signals, and combined to provide an output signal, which approximates the multiplication of the input signals. In an additional aspect of the present invention, an exponential signal is generated responsive to an input signal by maintaining a constant current in a first pair of series-connected junctions, thereby generating a first voltage

25   across the first pair of junctions; and driving a second pair of series-connected junctions with a voltage equal to the first voltage minus the voltage of the signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified schematic of an embodiment of a backbone of an RMS-DC

30   converter in accordance with the present invention.

FIG. 2 is a simplified schematic of an embodiment of an RMS-DC converter in accordance with the present invention, which utilizes a backbone similar to that of FIG. 1.

FIG. 3 is a schematic diagram of an alternative embodiment of an averaging circuit for the system of FIG. 2 in accordance with the present invention.

FIG. 4 is a schematic diagram of a second alternative embodiment of an averaging circuit for the system of FIG. 2 in accordance with the present invention.

FIG. 5 is a simplified schematic showing how the system of FIG. 2 can be configured for operation in a measurement mode in accordance with the present invention.

FIG. 6 is a simplified schematic showing how the system of FIG. 2 can be configured for operation in a controller mode in accordance with the present invention.

FIG. 7 is a simplified schematic showing how the system of FIG. 2 can be configured for operation in a measurement mode for measuring true power in a nonlinear load in accordance with the present invention.

FIG. 8 is a schematic diagram of a preferred embodiment of a wideband amplifier cell in accordance with the present invention suitable for use in a practical implementation of the circuit of FIG. 2.

FIG. 9 shows the large-signal gain function of the wideband amplifier cell of FIG. 8.

FIG. 10 is a schematic diagram of an embodiment of a four-quadrant multiplier in accordance with the present invention for use in a practical implementation of the circuit of FIG. 2.

FIG. 11 is a simplified schematic diagram of an embodiment of an averaging circuit in accordance with the present invention for a practical implementation of the circuit of FIG. 2.

FIG. 12 is a schematic diagram showing more details of a practical embodiment of the averaging circuit of FIG. 11.

FIG. 14 shows a preferred arrangement of differential attenuators and multipliers in accordance with the present invention for a practical implementation of the circuit of FIG. 2.

FIG. 14 is a simplified schematic diagram of an embodiment of a current source in accordance with the present invention suitable for use in the averaging circuit of FIGS. 11 and 12.

FIG. 15 is a schematic diagram showing more details of a practical embodiment of the current source of FIG. 14 in accordance with the present invention.

FIG. 16 is a schematic diagram of a conventional current mirror.

FIG. 17 illustrates the output characteristics of the current mirror of FIG. 16.

FIG. 18 is a schematic diagram showing a preferred embodiment of an averaging circuit for a practical implementation of an RMS-DC converter in accordance with the present invention.

FIG. 19 is a simplified schematic of an embodiment of an RMS-DC converter, which utilizes a single series of gain stages in accordance with the present invention.

FIG. 20 is a schematic diagram of an embodiment of a squaring cell in accordance with the present invention.

FIG. 21 is a schematic diagram of an embodiment of a four-quadrant multiplier in accordance with the present invention.

FIGS. 22 and 23 are simulation plots that illustrate the operation of the multiplier of FIG. 21.

FIG. 24 is a schematic diagram of an embodiment of a squaring cell in accordance with the present invention.

DETAILED DESCRIPTION

FIG. 1 is a simplified schematic of an embodiment of a backbone of an RMS-DC converter 8 in accordance with the present invention. The system of FIG. 1 includes a first chain or series of gain stages 12A, a second series of gain stages 12B, a first series of four quadrant multipliers M1, M2, . . . MN, and a second series of weighting multipliers W1, W2, . . . WN which only need to operate in two quadrants.

The first series of gain stages are connected in a cascade arrangement and generate a first series of progressively amplified signals V_{kA} (k = 1 . . . N) in response to the input voltage V_{IN}. Likewise, the second series of gain stages generate a second series of progressively amplified signals V_{kB} (k = 1 . . . N) in response to V_{IN}. The signals V_{1A} and V_{1B} are simply the input voltage V_{IN} (plus the noise from sources e_{nA} and e_{nB} as described below). The first series of multipliers are coupled to the first and second series of gain stages so that each multiplier Mk generates an output signal in response to the corresponding amplified signals V_{kA} and V_{kB}. Noise sources e_{nA} and e_{nB} are not a separate part of the system but are shown connected in series with the inputs of the first and second series of gain stages to represent the total input-referred thermal noise of each amplifier and to aid in explaining the effects of the thermal noise on the operation of the system of FIG. 1 as described below.

The outputs from the first series of multipliers are coupled to the second series of multipliers W1, W2, . . . WN. Each of the second multipliers Wk multiplies the output from the corresponding first multiplier by a corresponding weighting signal α_k to generate a weighted output current I_k. The value of the weighting signal α_k therefore acts as a weighting coefficient for the kth pair of amplified signals V_{kA} and V_{kB} and their product $V_{kA}V_{kB}$. The

series of weighted output currents $I_1, I_2, \ldots I_N$ from the multipliers Wk are then summed at a summing node N1 to generate the summed output current I_{OUT}. Each pair of corresponding multipliers M_k and W_k can be viewed as forming a combined multiplier/weighting stage.

An advantage of implementing the output signals I_k as currents is that they can be summed by simply combining the currents at a summing node N1. However, the present invention is not limited to embodiments in which the signals are realized as specific voltages or currents. For example, the multiplier/weighting stages could be implemented so that their output signals are in the form of voltages. In this case, the summing circuit could not be a simple summing node, but would need to be a more complicated circuit capable of summing several voltage signals. As another example, the input signal is shown as a voltage V_{IN}, however, implementations in which the input signal is applied as a current are possible. For purposes of explanation, the signals V_{IN}, V_{kA} and V_{kB} are hereinafter assumed to be voltages, and the weighted output signals I_k are hereinafter assumed to be current-mode signals.

The operation of the system of FIG. 1 will now be described by first considering the multipliers Mk and Wk. In the current-mode, the output current from Wk is the full product

$$I_k = \alpha_k V_{kA} V_{kB} \qquad \text{(Eq. 1)}$$

where α_k is correctly dimensioned. Assuming the input voltage V_{IN} is applied equally to both series of gain stages, and neglecting at this point the thermal noise of the circuit (represented by e_{nA} and e_{nB}), then $V_{kA} = V_{kB} = V_k$, and the weighted output of the k-th multiplier is

$$I_k = \alpha_k V_k^2 \qquad \text{(Eq. 2)}$$

The total output is thus

$$I_{OUT} = \alpha_1 V_1^2 + \alpha_2 V_2^2 + \ldots + \alpha_N V_N^2 = \sum_{k=1}^{N} \alpha_k V_k^2 \qquad \text{(Eq. 3)}$$

Since the amplification between each stage is G, and assuming the amplifiers are fully linear, the total output (again ignoring noise) is simply

$$I_{OUT} = \alpha_1 V_{IN}^2 + \alpha_2 (G V_{IN})^2 + \ldots + \alpha_N (G^{N-1} V_{IN})^2 = \sum_{k=1}^{N} \alpha_k \left(G^{k-1} V_{IN} \right)^2 \qquad \text{(Eq. 4)}$$

When the amplifiers are fully linear, V_{IN}^2 can be extracted as follows

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$$I_{OUT} = V_{IN}^2 \sum_{k=1}^{N} \alpha_k G^{2(k-1)} \qquad \text{(Eq. 5)}$$

showing that the system exhibits a square-law response to V_{IN}. However, in a practical system, the amplifiers 12A and 12B are not fully linear, but exhibit a limiting function as

5   described below with reference to FIGS. 8 and 9. In a practical amplifier, large inputs will cause later stages in each chain to limit.

To preserve the square-law response over a wide range of input voltages, the system is servoed by adjusting the weighting signals $\alpha_1, \alpha_2, \ldots \alpha_N$ so that most of the weighting signals are essentially zero, thereby disabling most of the multiplier/weighting stages. Those

10   left in operation respond to a linear replica of the inputs.

With the maximum input signal, the system servoes by adjusting the weighting signals so that only the first multiplier/weighting stage is enabled. That is, α_1 adjusts to a suitable full scale value α_{FS}, and $\alpha_2, \alpha_3, \ldots \alpha_N$ are all set to zero, or very nearly zero as described below. This prevents errors due to a loss of the square-law response, which would

15   be caused by limiting in the higher-numbered gain stages or multipliers. For smaller input signals, the system servoes by adjusting the weighting signals. Over the full input signal range, progressively higher numbered multiplier/weighting stages are enabled and then disabled as the signal decreases, until finally, with a very small input signal, the weighting signals are adjusted so that only the last multiplier/weighting stage is enabled, and the

20   remainder are disabled (i.e., $\alpha_1, \alpha_2, \ldots \alpha_{N-1}$ are all set to zero, and α_N is set to α_{FS}).

In a practical embodiment, the weighting signals are generated by an interpolator such as that described below with reference to FIG. 2 which does not completely turn off the weighting signals that are set to zero. Instead, they are reduced to a finite, but very small value. Also, the weighting signals "closest" to the large-valued signal may be significantly

25   greater than zero.

With a small input signal, the combined gain G^{N-1} of the N-1 amplifiers in each series of gain stages raises the small input signal to one of substantial amplitude $G^{N-1}V_{IN}$ and provides a usefully strong drive V_{NA} and V_{NB} to the last multiplier MN. Since only the last multiplier/weighting stage is enabled in response to a sufficiently small input signal, the

30   summed output current for that condition is:

$$I_{OUT} = \alpha_{FS}G^{2(N-1)}V_{IN}^2 \qquad \text{(Eq. 6)}$$

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The signals V_{kB} always have the same waveform as the input signal V_{IN} in theory. However, they are also affected in practice by the thermal noise generated internally within the system. This noise is represented in FIG. 1 by sources e_{nA} and e_{nB}, which have essentially the same RMS amplitude, but are fully uncorrelated. This noise affects the waveforms of

5   V_{kA} and V_{kB} by vector summation with V_{IN} as follows:

$$V_{kA} = G^{k-1}\sqrt{V_{IN}^2 + e_{nA}^2} \qquad \text{(Eq. 7)}$$

$$V_{kB} = G^{k-1}\sqrt{V_{IN}^2 + e_{nB}^2} \qquad \text{(Eq. 8)}$$

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Their cross-product after weighting is thus

$$I_{OUT} = \alpha_{FS} G^{2(k-1)}\sqrt{V_{IN}^2 + e_{nA}^2}\sqrt{V_{IN}^2 + e_{nB}^2} \qquad \text{(Eq. 9)}$$

15   which can be manipulated as follows:

$$I_{OUT} = \alpha_{FS} G^{2(k-1)} V_{IN}^2 \sqrt{1 + \left(\tfrac{e_{nA}}{V_{IN}}\right)^2}\sqrt{1 + \left(\tfrac{e_{nB}}{V_{IN}}\right)^2} \qquad \text{(Eq. 10)}$$

Then, using the approximation $\sqrt{1+x} \approx 1 + \dfrac{x}{2}$ when x is small:

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$$I_{OUT} = \alpha_{FS} G^{2(k-1)} V_{IN}^2 \left[1 + \left(\frac{e_{nA}}{2V_{IN}}\right)^2\right]\left[1 + \left(\frac{e_{nB}}{2V_{IN}}\right)^2\right] \qquad \text{(Eq. 11)}$$

which can be expanded to:

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$$I_{OUT} = \alpha_{FS} G^{2(k-1)} V_{IN}^2 \left[1 + \left(\frac{e_{nA}}{2V_{IN}}\right)^2 + \left(\frac{e_{nB}}{2V_{IN}}\right)^2 + \delta\right] \qquad \text{(Eq. 12)}$$

where δ is a very small residue, which can be ignored. Then,

$$I_{OUT} = \alpha_{FS} G^{2(k-1)} V_{IN}^2 \left[1 + \left(\frac{e_n}{V_{IN}}\right)^2\right] = \alpha_{FS} G^{2(k-1)}\left[V_{IN}^2 + e_n^2\right] \qquad \text{(Eq. 13)}$$

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where $e_{nA} = e_{nB} = e_n$, and δ is disregarded. The baseline output in the absence of any applied signal V_{IN} is then

$$I_{OUT} = \alpha_{FS} G^{2(k-1)} e_n^2 \qquad \text{(Eq. 14)}$$

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This always represents a miniscule instantaneous current, but with the dual amplifier scheme shown in FIG. 1, the cross-product averages asymptotically to zero over a sufficiently long interval because of the lack of coherence or correlation between the two noise signals e_{nA} and

5   e_{nB}. Furthermore, even when averaged over a finite, moderate interval, the effective noise bandwidth is that of a low-pass filter (described below) which is used to extract the average from I_{OUT}. This is in very strong contrast to a single amplifier having a squared noise $I_{OUT} = \alpha_{FS}G^{(N-1)}e_n$ wherein the net demodulated noise is that of the full-bandwidth signal, thereby imposing significant limitations on the dynamic range.

10   FIG. 2 is a simplified schematic of an embodiment of an RMS-DC converter 10 in accordance with the present invention. The system of FIG. 2 includes a backbone similar to that of FIG. 1, but each multiplier/weighting stage is implemented more efficiently as a single multiplier having a third input for scaling the multiplication in response to the corresponding weighting signal. Thus, the multiplication and weighting functions are combined in a single

15   cell. This cell will typically, though not necessarily, have a transconductance form, producing a current output. The outputs of the multipliers may therefore be coupled directly together at summing node N1 to generate the complete output current I_{OUT}.

        Another difference is that the lower numbered "gain" stages are now implemented as attenuators rather than amplifiers. For example, the lowest gain stage includes resistors R1A,

20   R1B, and R1C. The output signals from the attenuators are still referred to as amplified signals, although they are "amplified" with a gain of less than one. By implementing some of the gain stages as attenuators, the system can accommodate larger input signals. Therefore, the total number of weighting stages can be increased and the dynamic range of the system can be extended even further. It should also be noted that any suitable number of both the

25   attenuator-type gain stages and the amplifier-type gain stages can be used, including zero in either case, depending on the total input signal range required, and the gain or attenuation at each stage may have any suitable value. A typical value may be 10dB. Thus a total of ten gain and weighting stages provides an overall dynamic range of 100dB.

        The system of FIG. 2 also includes an averaging circuit and an interpolator 14. The

30   averaging circuit includes a capacitor C_{AVE}, which is coupled between the summing node N1 and power supply ground GND, a current source 16 which provides a reference current I_{REF} to the summing node N1, and an optional unity gain buffer amplifier 18 which buffers the voltage across C_{AVE} to provide the final output voltage V_{OUT}.

Referring again to FIG. 2, the interpolator 18 generates the weighting signals $\alpha_1, \alpha_2, \ldots \alpha_N$ in response to the control signal V_{CTRL}. In a preferred embodiment, the weighting signals are a series of continuous, overlapping Gaussian-shaped current pulses having a centroid whose location moves along the length of the interpolator as V_{CTRL} is varied so that

5   most of the weighting signals are nearly zero, but adjacent stages near the centroid are enabled to some extent. Also, the sum of all the weighting coefficients are typically, though not necessarily, a constant value α_{FS}:

$$\sum_{k=1}^{N} \alpha_k = \alpha_{FS} \qquad \text{(Eq. 15)}$$

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An interpolator capable of generating Gaussian-shaped current pulses meeting these requirements is disclosed in U.S. Patent No. 5,077,541 by the same inventor as the present application. In a preferred embodiment, the interpolator is of the type described in co-pending U.S. Patent Application Ser. No. 09/466,050, Attorney Docket No. 1482-117, filed

15   December 17, 1999 entitled "Interpolator Having Dual Transistor Ranks and Ratiometric Control" by the same inventor as the present application and which is incorporated by reference.

The use of Gaussian-shaped weighting signals produces a small sinusoidal ripple in the error between the actual response of the system and the response of an ideal RMS

20   measurement system. A linear interpolator such as that disclosed in U.S. Patent No. 5,432,478, also by the same inventor as the present application, could be used, but would result in a larger, quadratic ripple in the output function.

In the embodiment of FIG. 2, the gain stages 12A and 12B are implemented as "G/0" cells or "limiting" cells. That is, the incremental gain is G in response to very small signals,

25   but then falls off to zero as the signal increases in magnitude, as shown in FIG. 9. (These G/0 cells are also referred to as "A/0" cells in other patents and the inventor's literature). The gain stages can be implemented as simple bipolar pairs, in which case the large-signal function is a hyperbolic tangent function (tanh), and the incremental gain has a hyperbolic secant-squared ($sech^2$) form. However, it might be useful to provide a more linear gain

30   function, so multi-tanh cells can be used. Examples of multi-tanh cells are described in U.S. Patent Applications Ser. No. 09/212,089 filed December 15, 1998, which is now U.S. Patent No. 6,087,883, and Ser. No. 09/015,614 filed January 29, 1998, which is now U.S. Patent No. 6,084,472. Alternatively, the small-signal linearity can be improved using emitter degeneration or any other suitable technique. It should also be noted that the gain stages do

not need to be specifically of the limiting type in order for the principles of the present invention to be realized, although all practical amplifiers will eventually reach limiting operation.

As with the multipliers Mk and Wk in FIG. 1, the multipliers Mk in FIG. 2 are preferably implemented with current outputs to facilitate the summation of their weighted output currents I_k, which can be performed by a simple wire connection at a summing node rather than requiring a more complicated summing circuit. However, the present invention is not limited to embodiments having current outputs.

The system of FIG. 2 can be configured for operation in a measurement mode as shown in FIG. 5, in which case the signal to be measured is applied as the input V_{IN}, and the final output voltage V_{OUT} is used as a feedback signal by coupling it back to the interpolator as the control signal V_{CTRL}. With this connection, the system automatically servoes by adjusting the weighting signals until the average value of the output current I_{OUT} is equal to the reference current I_{REF}. The output voltage V_{OUT} then indicates the logarithm of the RMS value of the input signal, that is, the output is a linear-in-dB measure of the power of the input signal.

Alternatively, the system of FIG. 2 can be configured to operate as a controller. For example, it can be used to control the power delivered to an antenna 22 by an RF power amplifier 24 as shown in FIG. 6, in which case the final output voltage V_{OUT} is used to control the gain of the power amplifier, the input voltage V_{IN} is provided by a directional coupler 26 which samples the power from the amplifier, and a set-point signal is applied to the interpolator as the control signal V_{CTRL}. In this configuration, the feedback path is through the power amplifier and directional coupler. The system servoes until the power output from the amplifier corresponds to the value of the set-point signal. Again, the scaling relationship is linear-in-dB.

In the embodiments described above, a single input signal V_{IN} is applied equally to the first and second series of gain stages at input terminals IN_A and IN_B. This provides an accurate measure of the true power corresponding to the input signal V_{IN}, provided this voltage is measured across a linear load. However, by applying separate input signals to the first and second series of gain stages as shown in FIG. 7, the system of FIG. 2 can also be configured to measure the true power in a nonlinear load. Referring to FIG. 7, the voltage V_L across a load L is divided down by a resistive attenuator R1,R2 and applied as the first input signal IN_A to the first series of gain stages. A current shunt RS is connected in series with the load and generates a voltage, which is proportional to the current I_L through the load and

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used as the second input signal IN_B. In this configuration, the final output voltage V_{OUT} is used as a feedback signal by coupling it back to the interpolator as the control signal V_{CTRL}, to implement the measurement function.

If the circuit of FIG. 2 is used for high frequency (RF) applications, the averaging circuit must accommodate two types of averaging: RF ripple filtering of the carrier signal, and long-term averaging of the modulation envelope. The averaged signal must also be compared to a setpoint. In the averaging circuit shown in FIG. 2, the comparison and averaging functions are performed directly at connection of the reference signal I_{REF} and the averaging capacitor C_{AVE}. To prevent offset errors when used in the configurations shown in FIGS. 5-7, the averaging circuit should also accommodate an integration function to drive the error signal to zero. In the averaging circuit shown in FIG. 2, this is inherently performed in the averaging capacitor C_{AVE}, which integrates the error signal I_{ERR}. When the system has servoed to a particular input signal V_{IN}, $I_{OUT} = I_{REF}$ and $I_{ERR} = 0$, at which point the voltage on the capacitor remains at a stable value.

An alternative averaging circuit is shown in FIG. 3 where a resistor R is connected in parallel with the averaging capacitor C_{AVE}. Here, the averaging function is performed by resistor R and capacitor C_{AVE}. The comparison function is performed by the operational amplifier 20, which integrates the error signal V_{ERR} which is the difference between the voltage V_{AVE} across the capacitor and a reference voltage V_{REF}.

Another alternative averaging circuit is shown in FIG. 4. In the circuit of FIG. 4, the capacitor C_{AVE} is connected between the output terminal and noninverting input terminal of the operational amplifier 20. The noninverting input terminal of the op amp is also connected to node N1 and to V_{REF} through a resistor R. The inverting input terminal of the op amp is grounded. For the averaging circuit of FIG. 4 to work properly in an RMS-DC converter for RF applications, the op amp would need to be a very wide band amplifier, otherwise, some RF ripple filtering would need to be performed before the signal is feed to the amplifier.

In a practical monolithic realization, the gain stages, multipliers, and summing circuits shown in FIG. 2 would preferably be implemented with fully differential inputs and outputs as described below.

FIG. 8 is a schematic diagram of a preferred embodiment of an amplifier cell suitable for use in a practical implementation of the circuit of FIG. 2. The amplifier of FIG. 7 is based on the circuits disclosed in U.S. Patent Application Ser. No. 09/241,359 titled "Logarithmic Amplifier With Self-Compensating Gain For Frequency Range Extension"

filed January 29, 1999, which is now U.S. Patent No. 6,144,244, by the same inventor as the present application, and which is herein incorporated by reference.

The circuit of FIG. 8 is shown configured as one of the "A" series of amplifiers 12A and includes an differential pair of transistors Q1 and Q2 which receive the input signal $V_{kA}P$

5   and $V_{kA}M$, which is a differential form of one of the signals V_{kA} shown in FIG. 2. If the circuit of FIG. 8 was used for one of the "B" series of amplifiers, the inputs would be $V_{kB}P$ and $V_{kB}M$. The operation of a wideband amplifier such as that shown in FIG. 8 is described in detail in the above-referenced application Ser. No. 09/241,359, which is now U.S. Patent No. 6,144,244, but will be briefly summarized here for convenience.

10   Transistors Q1 and Q2 are biased by a current source transistor Q7 in response to a bias voltage V_B. The outputs from Q1 and Q2 drive emitter-follower transistors Q5 and Q6 through transistors Q3 and Q4 which act mainly as cascodes. By cross-connecting the bases of Q3 and Q4 to a fraction of the total output voltage, the fraction determined by the ratios R6/(R3+R6) and (equally) R5/(R4+R5), the effect of parasitic capacitance at the collectors of

15   Q3 and Q4 can be largely eliminated.

The differential output signal $V_{(k+1)A}P$, $V_{(k+1)A}M$ is provided at the emitters of emitter-follower transistors Q5 and Q6 which are biased by current source transistors Q8 and Q9 which are also driven by V_B. By sampling the load currents using R5 and R6, and also using positive feedback, the effect of the input capacitance of the following stage can be largely

20   eliminated. The circuit of FIG. 8 provides about 10dB of gain and is down -3dB at about 3.1GHz.

FIG. 9 shows the gain function of the wideband amplifier cell of FIG. 8. At low signal levels, the gain is linear and has a slope of "G". As the input signal level increases, the amplifier enters a limiting domain of operation at about ±E where the small signal gain

25   approaches zero.

FIG. 10 is a schematic diagram of an embodiment of a four-quadrant multiplier Mk for use in a practical implementation of the circuit of FIG. 2. The circuit of FIG. 10 includes a core of four transistors Q1-Q4 having their emitters connected together at a common node N2. A current source transistor Q5 sets up the weighting signal α_k in the form of a variable

30   bias current (or "tail current") to transistors Q1-Q4 at node N2 in response to the control signal V_{PSk} which is generated in the interpolator 18. The collectors of Q1 and Q4 are connected together at node N3 which is connected to output terminal 32, and the connectors of Q2 and Q3 are connected together at node N4 which is connected to output terminal 30.

The first "A" signal input terminal 34 is connected to the bases of Q1 and Q2 through resistors R1 and R3, respectively, while the second "A" input terminal 36 is connected to the bases of Q3 and Q4 through R5 and R7, respectively. Likewise, the first "B" signal input terminal 38 is connected to the bases of Q1 and Q3 through R2 and R6, respectively, while

5   the second "B" input terminal 40 is connected to the bases of Q2 and Q4 through R4 and R8, respectively.

The first differential input signal V_kAP, V_kAM, is applied to terminals 34 and 36, respectively, and the second differential input signal V_kBP, V_kBM, is applied to terminals 38 and 40, respectively. The differential output signal $I_kP - I_kM$, which is generated at terminals

10   30 and 32, is the result of the multiplication of the first and second input signals. By varying the weighting current α_k, which acts as the tail current for Q1-Q4, the transconductance of the entire multiplier is modulated so that the weighting signal acts as a third multiplying input that weights the output of the multiplier of FIG. 10 in proportion to the value of α_k.

The multiplier of FIG. 10 has a linear input range at its "A" and "B" inputs of about

15   ±40mV, beyond which, the behavior starts to enter a limiting domain of operation. A major advantage of the multiplier of FIG. 10 is that both inputs have the same common mode voltage, and also, the DC response is symmetric with respect to both inputs. The use of Q5 as a current source allows scaling of the multiplication operation in response to the weighting signal. More importantly, the AC response is also identical with respect to both. However,

20   any other type of variable current source can be used to achieve the third scaling input, or a fixed current source can be used if only a two-input multiplier with no scaling is required.

As discussed above, the interpolator 18 is preferably implemented as an interpolator having dual transistor ranks such as that described in co-pending U.S. Patent Application Ser. No. 09/466,050, Atty Docket No. 1482-117, filed December 17, 1999 entitled "Interpolator

25   Having Dual Transistor Ranks and Ratiometric Control" by the same inventor as the present application and which is incorporated by reference. If such an interpolator is used, then each transistor in the second rank of transistors in the interpolator also functions as the current source transistor Q5 in one of the multipliers of FIG. 10. The signal V_{PSk} is then a partially switched voltage signal generated by forcing a partially switched current I_{PSk} from the first

30   rank of transistors through a resistor connected to the base of Q5.

FIG. 11 is a simplified schematic diagram of an embodiment of an averaging circuit in accordance with the present invention for use in a practical realization of the circuit of FIG. 2. The circuit of FIG. 11 generates the final output voltage V_{OUT} in response to the differential input signal $I_{OUT}P, I_{OUT}M$ which is a differential version of the output signal I_{OUT}

of FIG. 2 obtained by separately summing the output signals I_kP and I_kM from the multipliers of FIG. 9.

Referring again to FIG. 11, resistors R3 and R4 provide a load for the currents $I_{OUT}P$ and $I_{OUT}M$. The op amp 20 forces Q9 to absorb the difference between $I_{OUT}P$ and $I_{OUT}M$.

5   The emitter current of Q9, which is a single-ended replica of the differential input current, is summed at node N5 with the current I_{REF} from current source 16. Capacitor C_{AVE}, which is also connected to node N5, integrates the error signal which is the difference between I_{REF} and the current through Q9. The voltage across C_{AVE} is then the final output voltage V_{OUT}, which is used to control the interpolator in the measurement mode.

10   FIG. 12 is a schematic diagram showing more details of a practical embodiment of the averaging circuit of FIG. 11. Referring to FIG. 12, resistors R3 and R4 provide a load for the currents $I_{OUT}P$ and $I_{OUT}M$, and also provide bias current for cascode transistors Q4 and Q5. Current source transistor Q1 establishes currents in Q2 and Q3, which in turn, establish an anchor voltage at the bases of Q4 and Q5 through beta compensation resistor R2. The

15   currents in Q4 and Q5 are thus replicas of the currents through Q2 and Q3. By scaling the area ratios between Q2,Q3 and Q4,Q5 the current through Q1 can be used to set the quiescent current through Q4 and Q5 in the absence of any differential between the input currents $I_{OUT}P$, $I_{OUT}M$. Any difference between $I_{OUT}P$ and $I_{OUT}M$ appears as a difference between the collector currents through Q4 and Q5. Therefore, the quiescent current must be large enough

20   to accommodate the largest expected difference between $I_{OUT}P$ and $I_{OUT}M$.

Transistors Q6 and Q7 form a current mirror which is optionally degenerated by resistors R6 and R7. Transistor Q10 provides beta compensation to the current mirror in a conventional manner. Transistors Q9 and Q11 maintain the current mirror in a balanced state because any difference between the currents $I_{OUT}P$ and $I_{OUT}M$ causes capacitor C1 to charge

25   or discharge through Q5 or the mirror which alters the current in Q9 and Q11. For the current in the mirror to remain balanced, Q9 must absorb the difference, and the result is a current through Q9 and Q11 which is proportional to the difference between $I_{OUT}P$ and $I_{OUT}M$.

The circuit of FIG. 12 converts the differential input current, which exists at a voltage

30   level close to the positive power supply rail V_P, to a single ended current through Q9 which can swing very close to the ground rail GND. The current source 16 should also be able to source the reference current I_{REF} at a voltage all the way down near GND. An embodiment of the current source 16 is described below with respect to FIGS 14 and 15. This allows the

output voltage V_{OUT} to swing close to GND which makes it easy to use V_{OUT} as the feedback voltage V_{CTRL} for driving the interpolator when the system is configured as a controller.

FIG. 18 is a simplified schematic diagram showing a preferred embodiment of an averaging circuit for a practical implementation of the system of FIG. 2. Referring to

5   FIG. 18, the averaging circuit includes load resistors R3 and R4 which convert the currents $I_{OUT}P$ and $I_{OUT}M$ to voltage signals which are input to an op amp 42 having differential current outputs connected to a current mirror 44. The capacitors across R3 and R4 perform high frequency ripple filtering. The op amp 42, which can be a simple gm cell, senses the voltage difference between the nodes N1P and N1M. Any imbalance in the voltage between

10   the nodes causes an imbalance in the current outputs of the gm cell. Since the current mirror 44 maintains equal currents in both sides, the differential output current from the op amp charges or discharges the filter capacitor C_{AVE}. The output signal V_{OUT}, which is preferably buffered by buffer amplifier 46, is generated across C_{AVE}. The reference current I_{REF} is provided by current source 16 which is connected across the nodes N1P and N1M.

15   An advantage of the circuit of FIG. 18 is that it charges and discharges the capacitor C_{AVE} at the same slew rate. This is in contrast to the circuit of FIG. 12 in which the capacitor is charged quickly by Q9, but only discharges at a rate established by the current I_{REF}.

FIG. 13 shows a preferred arrangement of differential attenuators and multipliers at the low numbered end of a practical embodiment of the backbone of the system of FIG. 2.

20   As is apparent from FIG. 13, the input resistors to the multiplier cells also function as part of the attenuator network. Therefore, the multipliers M1 and M2 shown in FIG. 13 only include the core of four transistors Q1-Q4 shown in FIG. 10.

In a practical embodiment of the system of FIG. 2, a dynamic range of over 100dB can be achieved using four pairs of attenuating gains stages and six pairs of amplifying gain

25   stages, each having 10dB of attenuation or gain. The values of the components should be chosen so that when the output current I_{OUT} is equal to the reference current I_{REF}, the multiplier or multipliers which are enabled by bias currents from the interpolator are operating in the accurate portion of their operating range. That is, they have not reached an output limiting range (as occurs in a logarithmic amplifier) but instead are acting essentially

30   as true squaring cells.

FIG. 14 is a simplified schematic of a current mirror suitable for use as the current source 16 in FIGS. 11 and 12, and the current mirror 44 of FIG. 18, and for other applications as well. Referring to FIG. 14, transistors Q12 and Q13 are configured much like in a basic current mirror. However, rather than connecting the collector of Q12 back to its base, the

15

collectors of Q12 and Q13 are connected to the noninverting and inverting inputs, respectively, of an op amp 28. The output of op amp 28 drives the bases of Q12 and Q13 and forces their collector voltages to track so that Q12 and Q13 both operate at the same collector voltage. Thus, the output current I_{REF} into the collector of Q13 precisely replicates the input current I_{IN} into the collector of Q12, even when the collector of Q13 swings all the way down to within a few millivolts of ground.

The benefits of the circuit of FIG. 14 can be better understood by considering the conventional current mirror Q18,Q19 shown in FIG. 16, and the output characteristic of transistor Q19 shown in FIG. 17. In the circuit of FIG. 16, the bases of Q18 and Q19 always operate at about a V_{BE} (~800mV) above GND. When the collector of Q19 is greater than a V_{BE} above GND, the current through the collector of Q19 tracks the current through the collector of Q18 reasonably well. However, when the collector voltage of Q19 drops below $V_{CE(SAT)}$, the base-collector junction of Q19 begins to saturate, thereby causing a very large error between the collector currents of Q18 and Q19. Saturation of Q19 also causes base current to be diverted from Q18 through the base-collector junction of Q19.

The circuit of FIG. 14, however, eliminates this problem by maintaining the collectors of Q12 and Q13 at the same voltage, all the way down to a within few millivolts of GND. Even though Q12 and Q13 are deeply in saturation when their collectors are much lower than $V_{CE(SAT)}$, all of the base current to Q12 and Q13 is provided by the op amp, so none of the base current required by Q12 is lost in the coupling to Q13.

A further advantage of the circuit of FIG. 14 is that, because Q12 and Q13 operate at the same collector voltage, the output impedance is infinite. An additional benefit is that the input offset voltage of the op amp 28 can be relatively high because a few millivolts of offset between the collectors of Q12 and Q13 do not have much effect on the operation of the circuit. Therefore, a simple inexpensive op amp can be utilized.

FIG. 15 is a schematic diagram showing more details of a practical embodiment of the current source of FIG. 14 in accordance with the present invention. In the circuit of FIG. 15, the op amp 28 is realized as a differential pair of PNP transistors Q14 and Q15 which are loaded by a current mirror formed by NPN transistors Q16 and Q17. Since the collectors of Q12 and Q13 are equal, the base currents in Q14 and Q15 are also equal, so there is no error due to base currents. Also, since the collectors of Q12 and Q13 are equal, the input current source 30 must have enough compliance to accommodate the expected voltage swing at the output node N5.

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Many of the advantages of the present invention can still be realized even with a single series of gain stages as shown in FIG. 19. The system of FIG. 19 is in many respects similar to those of FIGS. 1 and 2, but it only utilizes a single series of gain stages to generate a single series of amplified signals which are individually squared and weighted, and then

5   summed to generate an output signal. The squaring and weighting functions could be performed individually using a series of squaring/weighting stages, each having a squaring cell with a fixed scale factor and a multiplier for weighting the output from the squaring cell by multiplying it with a weighting signal. In a preferred embodiment, however, each squaring/weighting stage includes a single squaring cell (S1, S2, . . . SN) that can

10   simultaneously square and weight the signal from the gain stage responsive to a weighting signal as shown in FIG. 19.

The summed output signal I_{OUT} from the system of FIG. 19 is averaged and utilized in the same manner as that in FIGS. 1 and 2. As with the systems of FIGS. 1 and 2, the system of FIG. 19 can be implemented with any number of gain stages, and some of the lower

15   numbered gain stages can be attenuators rather than amplifiers. The system of FIG. 19 provides wide dynamic range power measurement at high operating frequencies, albeit without the benefit of uncorrelated noise cancellation obtained with a dual series of gain stages.

FIG. 20 shows an embodiment of a squaring cell in accordance with the present

20   invention suitable for use as one of the squaring cells S1, S2, . . . SN of FIG. 19. The squaring cell of FIG. 20 includes two exponential current generators 52 and 54, which generate output currents I_{C1} and I_{C2} that vary exponentially in response to the differential input voltage Vx which is the difference between the separate signals VxP and VxM. The first exponential current generator 52 includes a first emitter follower transistor Q1 which

25   receives the signal VxP at its base and has its emitter connected to the emitter of Q2 which is diode-connected. A current source 56 is connected to the collector and base of Q2 at node N6. A second emitter follower transistor Q3 receives the signal VxM at its base and has its emitter connected to the emitter of Q4 through an optional resistor R_S. The base of Q4 is connected to the base of Q2, and the collector of Q4 is connected to a summing node N7.

30   The current source 56 maintains a constant current I_0 through Q1 and Q2, thereby establishing a certain voltage across the series-connected base-emitter junctions of Q1 and Q2. Assuming Q1-Q4 has equal emitter areas, and neglecting the effect of R_S for now, the current through Q3 and Q4 is:

$$I_{C1} = I_0 \exp\left(\frac{-Vx}{2V_T}\right)$$ (Eq. 16)

The construction and operation of the second exponential current generator 54 is similar to that of generator 52, except that the bases of the emitter follower transistors Q5 and Q7 are connected to receive the opposite signals, so the current through Q7 and Q8 is:

$$I_{C2} = I_0 \exp\left(\frac{Vx}{2V_T}\right)$$ (Eq. 17)

The currents I_{C1} and I_{C2} are summed at node N7 to produce a final output current I_{SQR} which closely approximates the squared value of the input signal Vx. When the input signal Vx is zero, I_{SQR} has a quiescent offset value of $2I_0$. As the input signal increases in either direction, one of the exponential functions dominates, and I_{SQR} increases accordingly in the positive direction.

The square law approximation can be better understood by using Taylor series expansions for the exponential functions. First, the final output current I_{SQR} is:

$$I_{SQR} = I_0\left[\exp\left(\frac{Vx}{2V_T}\right) + \exp\left(\frac{-Vx}{2V_T}\right)\right]$$ (Eq. 18)

The expansions for the general exponential functions e^x and e^{-x} are:

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} \cdots$$ (Eq. 19)

and

$$e^{-x} = 1 - x + \frac{x^2}{2!} - \frac{x^3}{3!} + \frac{x^4}{4!} \cdots$$ (Eq. 20)

thus

$$e^x + e^{-x} = 2 + x^2 + \frac{x^4}{12} \cdots$$ (Eq. 21)

Using the expansion of Eq. 21 with Eq. 18 yields:

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$$I_{SQR} = I_0 \left[2 + \left(\frac{Vx}{2V_T} \right)^2 + \frac{1}{12} \left(\frac{Vx}{2V_T} \right)^4 \cdots \right]$$ (Eq. 22)

which shows that the form of the final output current I_{SQR} is dominated by the square term.

The squaring cell of FIG. 20 can be optimized for a particular application by including the resistors R_S which alter the currents I_{C1} and I_{C2} so as to soften the shape of the exponential functions, thereby providing a better approximation to a true square law behavior over a certain range of Vx. The inclusion of the resistors R_S diminishes the effect of the higher-order terms in the series expansion of Eq. 22.

When $R_S>0$, the outputs from the exponential current generators are not truly exponential, but instead, are less than that which would be generated by an exact exponential behavior. As used herein, the term exponential current generator refers not only to a circuit that generates a true exponential current, but also to a circuit that generates a "sub-exponential" function, that is, an output current which follows a nonlinear law which may be deliberately "softened", either by choice of transistor types or geometry, or by choice of bias currents, or by the inclusion of degeneration resistors R_S so as to result in an output that deviates from an ideal exponential function, as for example, for the purpose of more closely approximating an ideal square law when used for a squaring cell, or an ideal multiplicative law when used for a multiplier circuit as described below. Likewise, as used herein the term exponential current or signal refers not only to a true exponential current or signal, but also to an altered exponential current or signal. It should also be understood that the term exponential current generator also refers to any exponential function generator (e.g., voltage rather than current) that can generate exponential or sub-exponential functions which can be used to synthesize a squaring cell or multiplier.

To compensate for temperature variations, the currents I_0 should preferably be made proportional to absolute temperature (PTAT), and Vx is preferably arranged to also be PTAT--for example, as the output of a basic BJT gain stage.

An advantage of the circuit of FIG. 20 is that it can accommodate larger input voltage swings than other types of squaring circuits while still maintaining adequate square-law behavior. The peak output current I_{C1} in the circuit of FIG. 20 is not limited by the value of a bias current source as it is in the squaring cell disclosed in U.S. Patent Application No. 09/245,051 filed February 4, 1999, which is now U.S. Patent No. 6,204,719. Also, when the input signal and output current I_{C1} of the circuit of FIG. 20 become very large, the output

current I_{C1} can still behave according to an approximately exponential function, and the sum of two exponentials can provide a better approximation to a square law than the more-nearly linear behavior encountered with large signals in the squaring cell disclosed in U.S. Patent Application No. 09/256,640 filed February 24, 1999, which is now U.S. Patent No.

5   6,172,549. A further advantage of the circuit of FIG. 20 is that it can operate on a power supply voltage of 2 volts minimum for typical silicon transistors.

Many variations of the circuit of FIG. 20 are contemplated by the present invention. For example, in FIG. 20, the currents I_{C1} and I_{C2} are taken from the collectors of Q4 and Q8, and the collectors of Q3 and Q7 are shown connected to the power supply rail V_P.

10   Alternatively, the currents I_{C1} and I_{C2} could be taken from the collectors of Q3 and Q7, in which case, the collectors of Q4 and Q8 would be connected to GND. Although transistors Q1, Q3, Q5, and Q7 are shown as NPN devices and Q2, Q4, Q6 and Q8 are shown as PNP devices, other polarities and device types, including CMOS transistors, can be utilized. Also, the squaring cell of FIG. 20 is suitable not only for use as one of the squaring cells S1, S2, . .

15   . SN of FIG. 19, but for other applications as well.

Transistors Q1 and Q2, along with current source 56, in FIG. 20 form what can be referred to as a "constant current stack" because current source 56 maintains a constant current (or a PTAT current as discussed above, or a quasi-constant current as discussed below) through Q1 and Q2. Transistors Q3 and Q4 (and optionally R_S) form what can be

20   referred to as a variable current stack because the current I_{C1} varies in response to Vx. Different numbers of these stacks can be combined in accordance with the present invention to create additional useful circuits such as the four-quadrant multiplier described below with reference to FIG. 21.

If the currents I_0 from sources 56 and 58 in FIG. 20 are maintained at a constant level,

25   the squaring cell will have a fixed scaling factor. However, if the currents I_0 are made to vary in response to a control signal, such as one of the weighting signals α_k of FIG. 19, then the scale factor of the squaring cell will vary in response to the weighting signal, and the squaring and weighting functions can be performed simultaneously. In this case, the constant current I_0 can be referred to as a quasi-constant current, that is, even though the current can

30   be varied, the variation is generally independent of the input signal Vx. As used herein, the term constant current refers to both a constant current and a quasi-constant current.

FIG. 21 is a schematic diagram of an embodiment of a four-quadrant multiplier in accordance with the present invention. The multiplier of FIG. 21 is suitable for use as one of

the multipliers Mk in a practical implementation of the circuit of FIG. 2, as well as for numerous other applications.

The multiplier of FIG. 21 includes four exponential current generators, each having a constant current stack and a variable current stack similar to those in the squaring cell described above with reference to FIG. 20. However, the stacks in the multiplier circuit of FIG. 21 are cross-connected so as to generate two output currents I_{M1} and I_{M2}, the difference of which represents the four-quadrant multiplication of the input signals Vx and Vy.

The first exponential current generator generates the current I_{C1} and includes a constant current stack (Q1, Q2, CS1) driven by VxP and a variable current stack (Q3, Q4) driven by VyP. The second exponential current generator generates the current I_{C2} and includes a constant current stack (Q5, Q6, CS2) driven by VxM and a variable current stack (Q7, Q8) driven by VyM. The third exponential current generator generates the current I_{C3} and includes a constant current stack (Q9, Q10, CS3) driven by VyM and a variable current stack (Q11, Q12) driven by VxP. The fourth exponential current generator generates the current I_{C4} and includes a constant current stack (Q13, Q14, CS4) driven by VyP and a variable current stack (Q15, Q16) driven by VxM. The currents I_{C1} and I_{C2} are summed at node N9 to generate I_{M1}, while the currents I_{C3} and I_{C4} are summed at node N10 to generate I_{M2}. The currents I_{M1} and I_{M2} are converted to voltages by resistors R_{L1} and R_{L2} to generate the final output voltage V_M.

As with the squaring cell of FIG. 20, multiplying behavior of the multiplier of FIG. 21 can be better understood by using Taylor series expansions for the exponential functions. Taking the final output signal as a current I_M, which is the difference between the currents I_{M1} and I_{M2}, and using x to denote $Vx/2V_T$ and y to denote $Vy/2V_T$, the final output current I_M is:

$$I_M = I_0[\exp(x+y) + \exp(-x-y) - \exp(x-y) - \exp(y-x)] \qquad \text{(Eq. 23)}$$

$$= I_0(e^x - e^{-x})(e^y - e^{-y}) \qquad \text{(Eq. 24)}$$

Using the expansions for $(e^x - e^{-x})$ and $(e^y - e^{-y})$ yields:

$$I_M = I_0 \left[2x + \frac{x^3}{3} + \cdots \right]\left[2y + \frac{y^3}{3} + \cdots \right] \qquad \text{(Eq. 25)}$$

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$$= \quad I_0\left[4xy + \frac{2}{3}\left(xy^3 + yx^3\right) + \cdots\right] \qquad \text{(Eq. 26)}$$

The cubic terms are unimportant provided x and/or y are less than 1 (which requires Vx and/or Vy to be less than $2V_T$, that is, less than about 52mV at T=27°C), so the final output current is dominated by the "xy" term. If the resistors R_S are included, the exponential functions are modified so as to soften the response to large values of Vx and Vy, while not seriously degrading the accuracy for more moderate values.

As with the squaring cell of FIG. 20, the curve-shaping resistors R_S in the multiplier of FIG. 21 are optional, and the currents I_{C1} through I_{C4} can be obtained from either end of the variable current stacks. If no gain scaling is used, I_0 should preferably be made PTAT to compensate for temperature variations. Also, the current sources can be designed to vary I_0 in response to a weighting signal α_k so the multiplying and weighting functions can be performed simultaneously when the multiplier of FIG. 21 is used as one of the multipliers Mk in the circuit of FIG. 2.

An advantage of the multiplier of FIG. 21 is that it can accommodate input signals up to about ±300mV at T=27°C. FIGS. 22 and 23 are simulation plots that illustrate the operation of the multiplier of FIG. 21 where I0 = 100μA and the NPN and PNP transistors have 0.8μm by 10μm emitters. FIG. 22 shows the output voltage V_M as Vx is varied between -400mV and +400mV for several different values of Vy. As is apparent from FIG. 22, the multiplier maintains reasonably good linearity until the input signal reaches about ±300mV.

FIG. 23 shows the incremental gain of the multiplier vs. frequency for Vy = 50mV, 100mV, 150 mV, and 200mV. The -3dB points for these voltages are at 1.86GHz, 2.21GHz, 2.59GHz, and 2.87GHz, respectively.

When a squaring cell is used to measure a small input signal, the standing current (zero-signal current) should be as small as possible because, otherwise, the output signal is difficult to discern from the standing current. Additionally, when two squaring cells are used together, high standing currents exacerbate device mismatches and jeopardize the balance between the cells.

In the circuit of FIG. 20, the reduction in standing current that can be achieved by simply lowering I_0 is limited by the fact that R_S cannot be made too large. Otherwise, the output of the squaring cell will become very linear in response to large input signals and the square-law behavior is lost.

This problem is overcome by the introduction of collector resistors R_C in series with the collectors of Q2 and Q6 as shown in FIG. 24. The bases of Q2 and Q6 are then connected between R_C and the corresponding current source. The voltage drop across the collector resistors, which serve to back-bias the entire arrangement, is independent of the

5   input signal. By adding this precise voltage drop, the standing current can be reduced without significantly compromising the response to large input signals. Thus, the output signal caused by very small input signals can easily be discerned.

If the voltage drop across R_C is made too large, the squaring cell will not respond accurately to small input signals. An optimum value will typically be about a few V_T, where

10   V_T is the thermal voltage (~26mV at 300°K).

Having described and illustrated the principles of the invention in preferred embodiments thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. For example, although the principles of the present invention have been illustrated with embodiments implemented with bipolar

15   junction transistors (BJTs), it will be apparent that they can also be realized in different technologies, including CMOS, usually with fairly minor changes to the detailed design. We claim all modifications and variations coming within the spirit and scope of the following claims.